CLAIM SUMMARY

1. (Presently amended) A method of forming a capacitor in an integrated circuit, the method comprising:

forming a first non-single-crystalline layer on a gate dielectric layer on a surface of a substrate of an integrated circuit;

forming a capacitor dielectric layer on the first non-single-crystalline layer;

forming a second non-single-crystalline layer on the capacitor dielectric layer;

removing portions of the second non-single-crystalline layer to define a top plate of the capacitor;

removing portions of the capacitor dielectric layer to define a dielectric of the capacitor; and

removing portions of the first non-single-crystalline layer to define a bottom plate of the capacitor after a top plate is defined on the gate dielectric layer.

2. (Original) The method according to claim 1, wherein portions of the first non-single-crystalline layer are removed to simultaneously define a gate of a transistor of the integrated circuit.

3. (Original) The method according to claim 1, including forming a mask over the second non-single-crystalline layer with an opening and etching to remove the portions of the second non-single-crystalline layer.

4. (Original) The method according to claim 3, including etching to remove the portions of the capacitor dielectric layer using the mask.

5. (Original) The method according to claim 1, including using the top plate as a mask and etching to remove the portions of the capacitor dielectric layer.

6. (Original) The method according to claim 5, wherein using the top plate as a mask and etching is performed one of before and after removing the portions of the first non-single-crystalline layer.

7. (Original) The method according to claim 1, including forming a mask over the top plate and exposed portions of one or more of the first non-single-crystalline layer and the capacitor dielectric layer with an opening and etching to remove the portions of one or more of the first non-single-crystalline layer and the capacitor dielectric layer.

8. (Original) The method according to claim 7, wherein the masking and etching removes portions of the capacitor dielectric layer and the first non-single-crystalline layer and defines the bottom plate.

9. (Original) The method according to claim 8, subsequent to the masking and etching, using the top plate as a mask and etching to remove additional portions of the capacitor dielectric layer to define the dielectric of the capacitor.

10. (Original) The method according to claim 7, wherein the mask covers the defined capacitor dielectric, and the etching removes portions of and defines the bottom plate.

11. (Original) The method according to claim 7, wherein the masking and etching removes portions of the capacitor dielectric layer and the first non-single-crystalline layer and defines the capacitor dielectric and defines the bottom plate.

12. (Original) The method according to claim 11, including forming a top dielectric layer over the defined first and second plates and the capacitor dielectric and forming contact vias to the first plate through the top dielectric and the capacitor dielectric and to the second plate through the top dielectric.

removed to define a bottom gate on the gate dielectric layer. Thus, Claim 1 and its dependent claims are allowable over Chi.

Upon review of Claims 1-12 it is evident that claims 1-12 are allowable over the art of record and thus the passage of this case to issue is respectfully solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to the Account of Barnes & Thornburg LLP, Deposit Account No. 02-1010 (33851/41886).

Respectfully submitted,
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